

WHAT IS CLAIMED IS:

1. A random access memory (RAM) device comprising:
a memory array;
a level detector monitoring a source voltage and providing a level signal representative of a voltage range of the source voltage;
an off-chip driver (OCD) associated with the memory array and providing an output signal having at least one operating parameter, wherein the OCD adjusts the at least one operating parameter by adjusting a magnitude of at least one impedance based on the level signal.
2. The memory of claim 1, wherein the device is a dynamic random access device (DRAM).
3. The memory of claim 1, wherein each impedance of the plurality of impedances comprises a plurality of transistors.
4. The memory of claim 1, wherein the at least one operating parameter comprises a current.
5. The memory of claim 4, wherein the OCD further comprises:
a first impedance of the plurality of impedances comprising a plurality of transistors coupled in parallel between the output node and the source voltage;
and
a second impedance of the plurality of impedances comprising a plurality of transistors coupled in parallel between the output node and a reference node.
6. The memory of claim 1, wherein the at least one operating parameter comprises a slew-rate.
7. The memory of claim 6, wherein the OCD further comprises:

a first transistor coupled between the output node and the source voltage and having a control gate;

a second transistor coupled between the output node and a reference node and having a control gate;

a first impedance of the plurality of impedances comprising a plurality of transistors coupled between the control gate of the first transistor and a power supply; and

a second impedance of the plurality of impedances comprising a plurality of transistors coupled between the control gate of the second transistor and a reference node.

8. A dynamic random access memory device comprising:

a memory array;

a level detector monitoring a source voltage and providing a level signal representative of a voltage range of the source voltage; and

an off-chip driver (OCD) associated with the memory array, the OCD receiving a data signal having a first and a second state and providing at an output node an output signal having a current level, wherein the OCD couples the output node to the source voltage via a first impedance when the data signal has the first state and to a reference node via a second impedance when the data signal has the second state, and wherein the OCD adjusts the current level by adjusting a magnitude of the first impedance and a magnitude of the second impedance based on the level signal.

9. The memory of claim 8, wherein the level signal comprises a low level signal and a high level signal, wherein the low level signal has a first state when the source voltage is less than the voltage range and second state when the source voltage is within the voltage range and the high level signal has a first state when the source voltage is greater than the voltage range and a second state when the source voltage is within the voltage range.

10. The memory of claim 9, wherein the OCD includes a logic block receiving the data signal and an enable signal having an active state, and providing a pull-up enable signal having an active state when the enable signal has the active state and the data signal has the first state, and providing a pull-down enable signal having an active state when the enable signal has the active state and the data signal has the second state.

11. The memory of claim 10, wherein the logic block comprises:
an AND-gate receiving the data signal at a first input and the enable signal at a second input, and providing the pull-up enable signal at an output;
an inverter receiving the enable signal at an input and having an output;
and
an OR-gate receiving the data signal at a first input, coupled to the inverter output at a second input, and providing the pull-down enable signal at an output.

12. The memory of claim 10, wherein the OCD further comprises:
a pull-up circuit configured to couple the output node to the source voltage via the first impedance when the pull-up enable signal has the active state, and configured to increase the magnitude of the first impedance when the high level signal has the first state and to decrease the magnitude of the first impedance when the low level signal has the first state; and
a pull-down circuit configured to couple the output node to the source voltage via the second impedance when the pull-down enable signal has the active state, and configured to increase the magnitude of the second impedance when the high level signal has the first state and to decrease the magnitude of the second impedance when the low level signal has the first state.

13. The memory of claim 12, wherein the first impedance comprises a first plurality of transistors coupled in parallel between the source voltage and the output node and the second impedance comprises a second plurality of

transistors coupled in parallel between the output node and the reference node, and wherein the pull-up and pull-down circuits adjust the magnitudes of the first and second impedances by turning on varying numbers of transistors based on the high and low level signals.

14. The memory of claim 13, wherein the pull-up circuit comprises
- an first inverter receiving the second level signal at an input and having an output;
 - a first AND-gate receiving the pull-up enable signal at a first input, having a second input coupled to the output of the first inverter, and having an output;
 - a second AND-gate receiving the pull-up enable signal at a first input, the first level signal at a second input, and having an output;
 - a second inverter receiving the pull-up enable signal at an input and providing a first pull-up signal at an output;
 - a third inverter having an input coupled to the output of first AND-gate and providing a second pull-up signal at an output; and
 - a fourth inverter having an input coupled to the output of the second AND-gate and providing a third pull-up signal at an output.

15. The memory of 14, wherein the first impedance comprises:
- a first PMOS transistor having a source coupled to the source voltage, a drain coupled to the output node; and a gate receiving the first pull-up signal;
 - a second PMOS transistor having a source coupled to the source voltage, a drain coupled to the output node; and a gate receiving the second pull-up signal;
 - a third PMOS transistor having a source coupled to the source voltage, a drain coupled to the output node; and a gate receiving the third pull-up signal.

16. The memory of 13, wherein the pull-down circuit comprises:

a first inverter receiving the first level signal at an input and having an output;

a first OR-gate receiving the pull-down enable signal at a first input, the second level signal at a second input, and having an output;

a second OR-gate receiving the pull-down enable signal at a first input, having a second input coupled to the output of the first inverter, and having an output;

a second inverter receiving the pull-down enable signal at an input and providing a first pull-down signal at an output;

a third inverter having an input coupled to the output of the first OR-gate and providing a second pull-down signal at an output; and

a further inverter having an input coupled to the output of the second OR-gate and providing a third pull-down signal at an output.

17. The memory of 16, wherein the second impedance comprises:

a first NMOS transistor having a drain coupled to the output node, a source coupled to a reference node, and a gate receiving the first pull-down signal;

a second NMOS transistor having a drain coupled to the output node, a source coupled to a reference node, and a gate receiving the second pull-down signal;

a third NMOS transistor having a drain coupled to the output node, a source coupled to a reference node, and a gate receiving the third pull-down signal.

18. A dynamic random access memory device (DRAM) comprising:

a memory array;

a level detector monitoring a source voltage and providing a level signal representative of a voltage range of the source voltage; and

an off-chip driver (OCD) associated with the memory array, the OCD receiving a data signal having a first and a second state and providing an

output node an output signal having a slew rate, wherein the OCD couples the source node to the source voltage via a first output switch having a control gate when the data signal has the first state and to a reference node via a second output switch having control gate when the data signal has the second state, and wherein the OCD adjusts the slew rate by adjusting a magnitude of a first impedance coupled between the control gate of the first output switch and a power supply and a magnitude of a second impedance coupled between the control gate of the second output switch and a reference node based on the level signal.

19. The memory of claim 18, wherein the level signal comprises a low level signal and a high level signal, wherein the low level signal has a first state when the source voltage is less than the voltage range and second state when the source voltage is within the voltage range and the high level signal has a first state when the source voltage is greater than the voltage range and a second state when the source voltage is within the voltage range.

20. The memory of claim 19, wherein the OCD includes a logic block receiving the data signal and an enable signal having an active state, and providing a pull-up enable signal having an active state when the enable signal has the active state and the data signal has the first state, and providing a pull-down enable signal having an active state when the enable signal has the active state and the data signal has the second state.

21. The memory of claim 20, wherein the logic block comprises:
an AND-gate receiving the data signal at a first input and the enable signal at a second input, and providing the pull-up enable signal at an output;
an inverter receiving the enable signal at an input and having an output;
and

an OR-gate receiving the data signal at a first input, coupled to the inverter output at a second input, and providing the pull-down enable signal at an output.

22. The memory of claim 20, wherein the OCD further comprises:

a pull-up circuit configured to turn-on the first output switch when the pull-up enable signal has the active state, and configured to increase the magnitude of the first impedance when the high level signal has the first state and to decrease the magnitude of the first impedance when the low level signal has the first state; and

a pull-down circuit configured to turn-on the second output switch when the pull-down enable signal has the active state, and configured to increase the magnitude of the second impedance when the high level signal has the first state and to decrease the magnitude of the second impedance when the low level signal has the first state.

23. The memory of claim 22, wherein the first impedance comprises a first plurality of transistors coupled between the control of the first output switch and the power supply and the second impedance comprises a second plurality of transistors coupled in between the control gate of the second output switch and the reference node, and wherein the pull-up and pull-down circuits adjust the magnitudes of the first and second impedances by turning on varying numbers of transistors based on the high and low level signals.

24. The memory of claim 23, wherein the first switch comprises a PMOS switch having the control gate, a source coupled to the source voltage, and a drain coupled to the output node, and the second switch comprises an NMOS switch having the control gate, a source coupled to the reference node, and a drain coupled to the output node.

25. The memory of claim 24, wherein the pull-up circuit comprises:

a first inverter receiving the pull-up enable signal at an input and providing a pull-up signal at an output;

a second inverter receiving the second level signal at an input and having an output; and

the first impedance, the first impedance comprising:

a first NMOS transistor having a gate receiving the pull-up enable signal, a drain coupled to the output of the first inverter, and having a source;

a second NMOS transistor having a gate receiving the pull-up enable signal, a drain coupled to the output of the first inverter, and having a source;

a third NMOS transistor having a gate coupled to the output of the second inverter, a drain coupled to the source of the first NMOS transistor, and a source coupled to a reference node; and

a fourth NMOS transistor having a gate receiving the first level signal, a drain coupled to the source of the second NMOS transistor, and a source coupled to the reference node.

26. The memory of claim 24, wherein the pull-down circuit comprises:
- a first inverter receiving the pull-down enable signal at an input and providing a pull down signal at an output;
- a second inverter receiving the first level signal at an input and having an output; and
- the second impedance, the second impedance comprising:
- a first PMOS transistor having a gate coupled to the output of the second inverter, a source coupled to the source voltage; and having a drain;
- a second PMOS transistor having a gate receiving the second level signal, a source coupled to the source voltage, and having a drain;

a third PMOS transistor having a gate receiving the pull-down enable signal, a source coupled to the drain of the first PMOS transistor, and a drain coupled to the output of the first inverter; and

a fourth PMOS transistor having a gate receiving the pull-down enable signal, a source coupled to the drain of the second PMOS transistor, and a drain coupled to the output of the output of the first inverter.

27. A method of adjusting a current level of an output signal of an off-chip driver in a dynamic random access memory device, the method comprising:
providing a level signal representative of a voltage range of a source voltage;
receiving a data signal having a first state and a second state;
providing the output signal at an output node by coupling the output node to the source voltage via a first impedance when the data signal has the first state and to a reference node via a second impedance when the data signal has the second state; and
varying a magnitude of the first impedance and a magnitude to the second impedance based on the level signal.
28. A method of adjusting a slew rate of an output signal of an off-chip driver in a dynamic random access memory device, the method comprising:
providing a level signal representative of a voltage range of a source voltage;
receiving a data signal having a first state and a second state;
providing the output signal at an output node by coupling the output node to the source voltage via a first switch having a control gate when the data signal has the first state and by coupling the output node to a reference node via a second switch having a control gate when the data has the second state;

providing a first impedance between the control gate of the first switch and a power supply and a second impedance between the control gate of the second switch and a reference node; and

varying a magnitude of the first impedance and a magnitude of the second impedance based on the level signal.